

<b>Notice of Allowability</b>	Application No.	Applicant(s)	
	10/670,331	KANEDA ET AL.	
	Examiner	Art Unit	
	Belur V Keshavan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTO-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to 09/10/2004.
2.  The allowed claim(s) is/are 1-26.
3.  The drawings filed on 26 September 2003 are accepted by the Examiner.
4.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All
  - b)  Some\*
  - c)  None
 of the:
  1.  Certified copies of the priority documents have been received.
  2.  Certified copies of the priority documents have been received in Application No. 10/366520.
  3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached  
 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of  
 Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

#### Attachment(s)

1.  Notice of References Cited (PTO-892)
2.  Notice of Draftsperson's Patent Drawing Review (PTO-948)
3.  Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
 Paper No./Mail Date already sent w/6/19/04 action
4.  Examiner's Comment Regarding Requirement for Deposit  
 of Biological Material
5.  Notice of Informal Patent Application (PTO-152)
6.  Interview Summary (PTO-413),  
 Paper No./Mail Date \_\_\_\_\_.
7.  Examiner's Amendment/Comment
8.  Examiner's Statement of Reasons for Allowance
9.  Other \_\_\_\_\_.

  
 MATTHEW SMITH  
 SUPERVISORY PATENT EXAMINER  
 TECHNOLOGY CENTER 2800

**DETAILED ACTION**

***Status Of Claims***

Claims 1-26 are currently pending in the application.

***Examiner's Statement As To The Reasons For Allowance***

In reply to the Office Action of June 17, 2004, Applicants have submitted express abandonment and there by officially abandoning allowed parent application No. 10/366,520.

During an interview on September 27, 2004 with Applicants' attorney, Mr. Andrew Harry, Examiner was informed that issue fee for the parent application No. 10/366,520 has not been paid.

In view of the abandonment of the parent application No. 10/366,520, the provisional rejection of claims 1-8, 11 and 14-22 under 35 U.S.C. 101 is withdrawn.

Claims 1-26 are allowed.

The following is an examiner's statement of reasons for allowance:

The claimed invention is related to a semiconductor substrate used in a semiconductor device (in claims 1-4), a semiconductor device (in claims 5-13), a method of manufacturing a semiconductor substrate (in claims 14-18) and a method of manufacturing a semiconductor device (in claims 19-26).

The primary reason for the allowance of claims 1-4, 14-18, 5-13 and 19-25 is inclusion therein, in combination as currently claimed of the limitation of a semiconductor substrate, a method of manufacturing the semiconductor substrate, a semiconductor device comprising the semiconductor substrate and a method of manufacturing the semiconductor device in the substrate. The limitation of a semiconductor substrate, a method of manufacturing the

semiconductor substrate, a semiconductor device comprising the semiconductor substrate and a method of manufacturing the semiconductor device on the substrate comprise **inter alia** the following: a substrate of a first conductivity type having a first main surface and a second main surface which are opposed to each other; an impurity diffusion layer of a second conductivity type different from the first conductivity type being formed in the first main surface by diffusing an impurity; and an impurity diffusion region of the second conductivity type formed partially in the second main surface by diffusing an impurity, having a bottom surface reaching the impurity diffusion layer and surrounding a portion of the substrate which has the first conductivity type, wherein the portion surrounded by the impurity diffusion region is defined as an element formation region; forming partially in the second main surface in the element formation region a first impurity region of the second conductivity type serving as a base of the transistor; forming partially in the second main surface in the first impurity region a second impurity region of the first conductivity type serving as an emitter of the transistor; forming a gate electrode on the second main surface with a gate insulating film interposed there between above the first impurity region positioned between the second impurity region and a portion of substrate which has the first conductivity type; and forming a first local lifetime region by implanting proton into a substantially middle region with respect to a film thickness direction of the portion of the substrate which has the first conductivity type from the first main surface through the impurity diffusion layer.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BVK.  
September 28, 2004.

Belur V. Keshavan.  
Examiner. Art Unit 2825.



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